Future of Nano CMOS Technology

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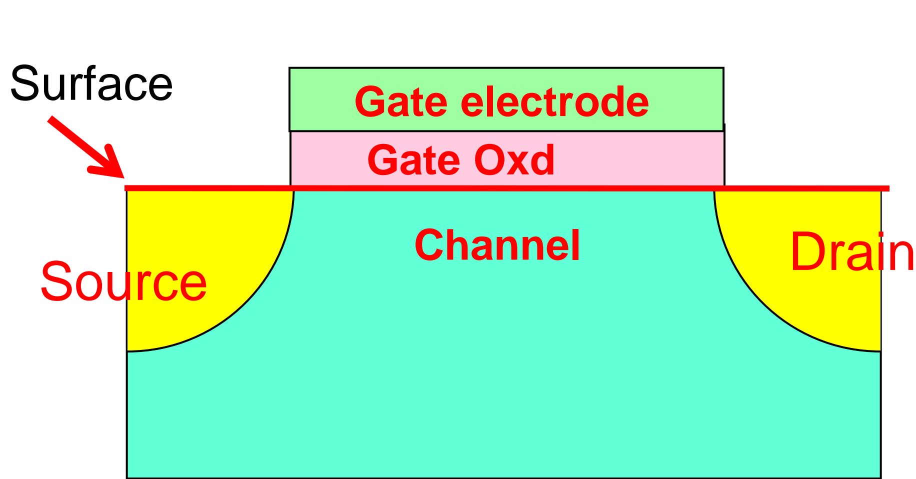
First Computer Eniac: made of huge number of vacuum tubes 1946

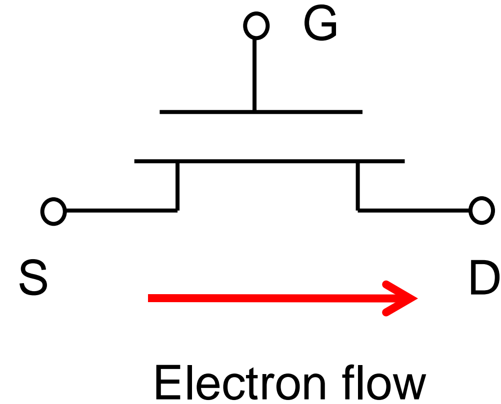
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

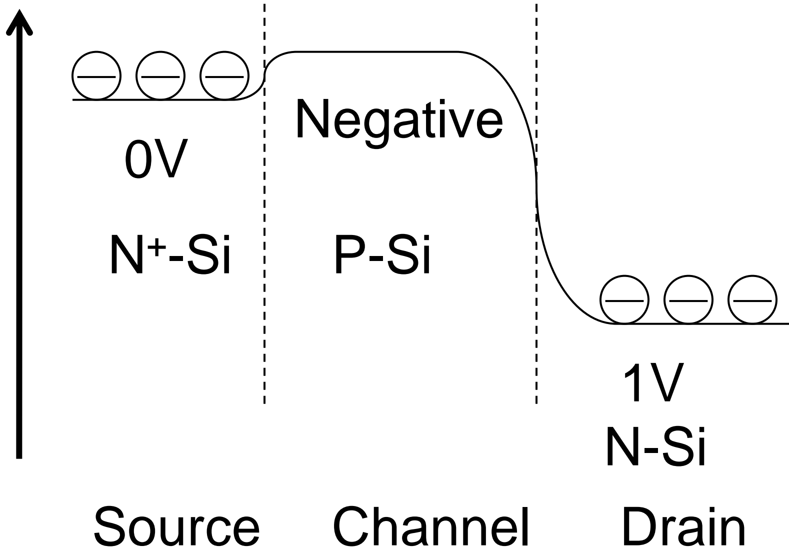
Mechanism of MOSFET (Metal Oxide Semiconductor Field Effect Transistor)



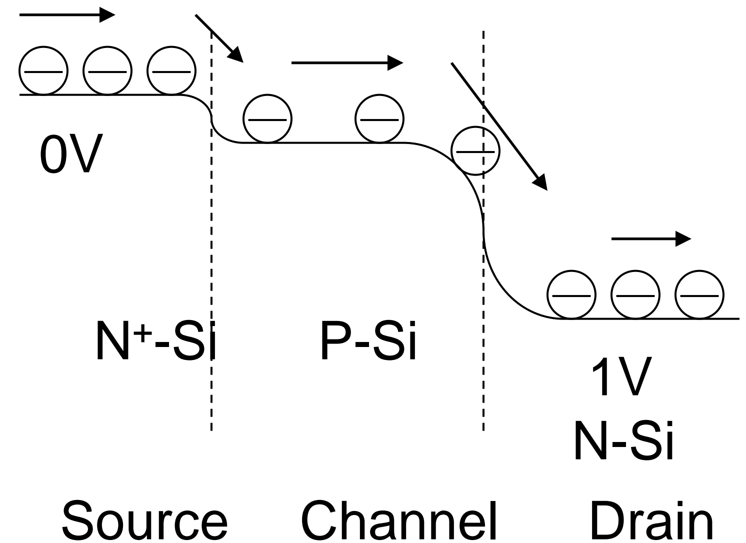


0 bias for gate

Surface Potential (Negative direction)



Positive bias for gate



1960: First MOSFET by D. Kahng and M. Atalla

Top View

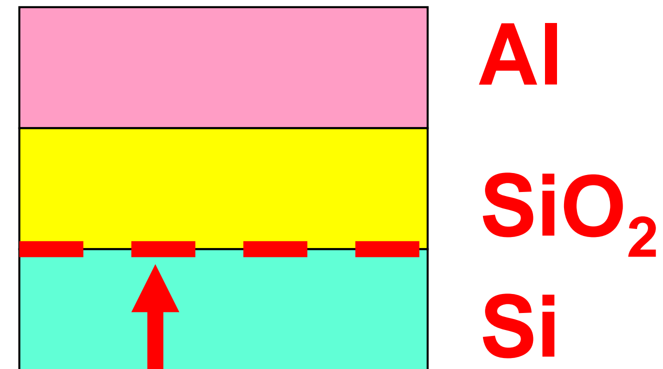
Si

Source

Al Gate

Drain

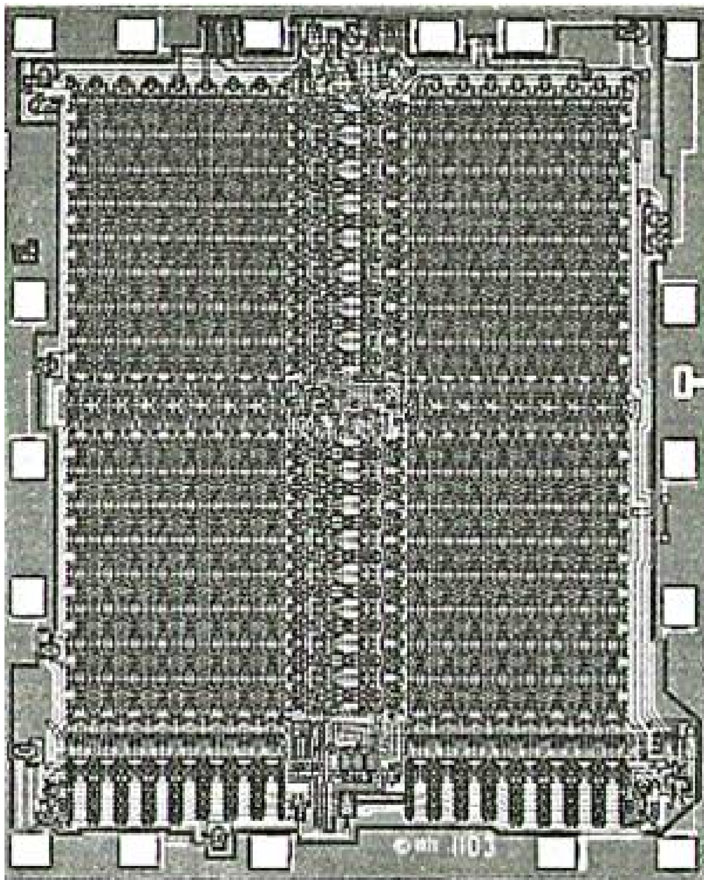
Si



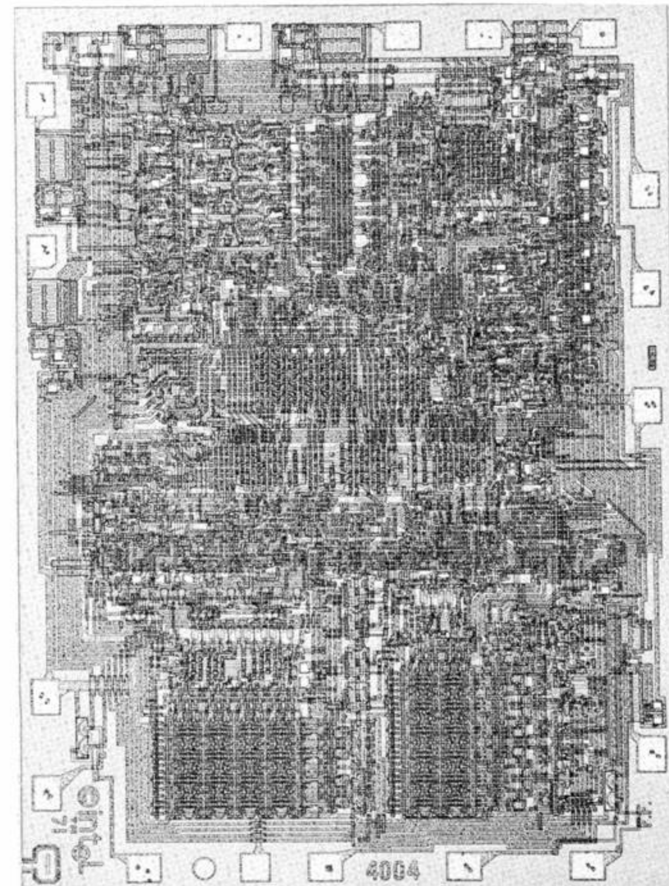
Si/SiO_2 Interface is exceptionally good

1970,71: 1st generation of LSIs

1kbit DRAM Intel 1103



4bit MPU Intel 4004



2011

Most recent SD Card

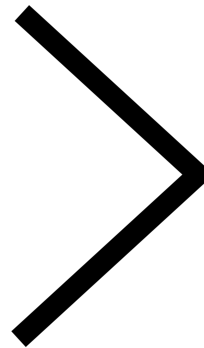
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population：6 Billion
Brain Cell：10～100 Billion
Stars in Galaxy：100 Billion

Most Recent SD Card



2.4cm X 3.2cm X 0.21cm

Volume：1. 6cm^3 Weight：2g

Voltage：2.7 - 3.6V

Old Vacuum Tube：
5cm X 5cm X 10cm, 100g,100W

1Tbit = 10k X10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km^3 = 0.25X10^{12}cm^3

Weight = 0.1 kgX10^{12} = 0.1X10^{9}ton = 100 M ton

Power = 0.1kWX10^{12}=50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW

So, progress of IC technology is most important for the power saving!

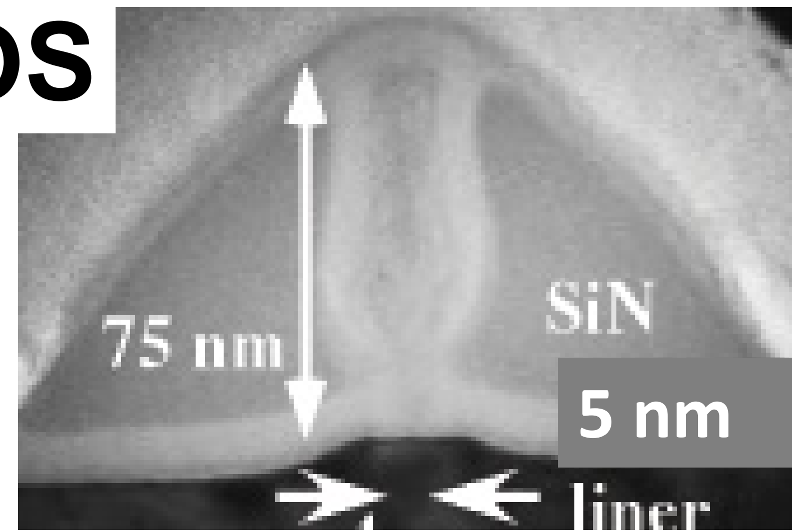
Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

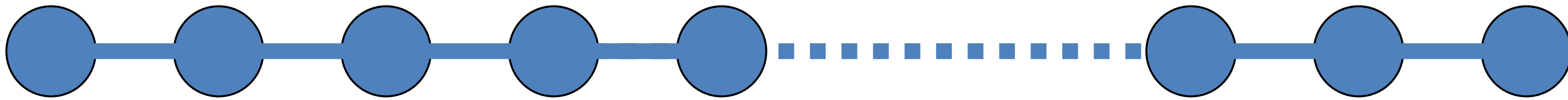
In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

5 nm gate length CMOS

Is a Real Nano Device!!

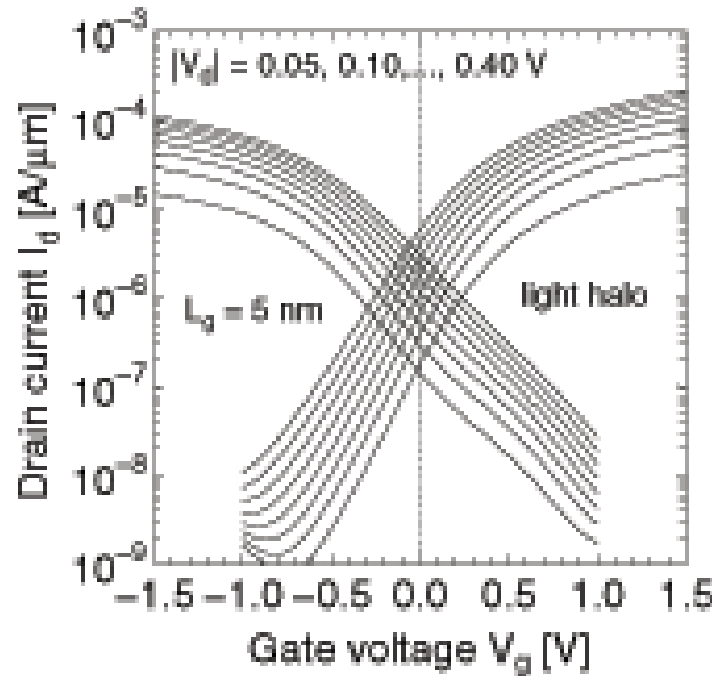


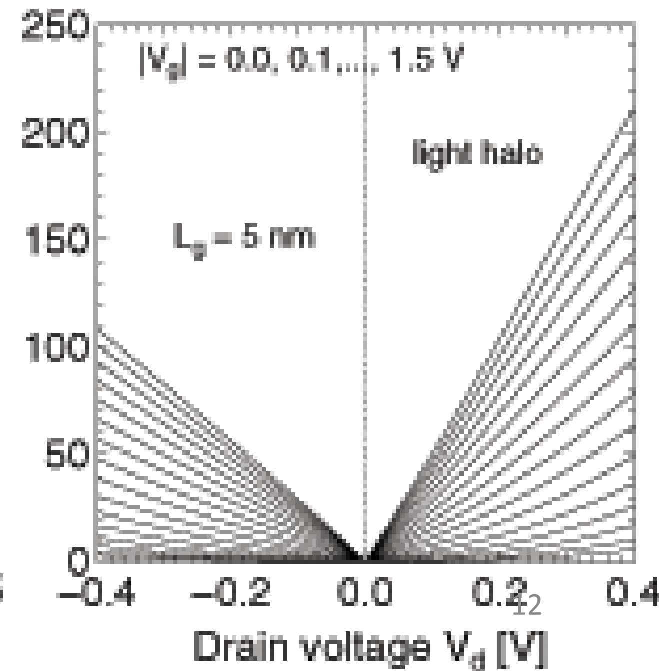
Length of 18 Si atoms



H. Wakabayashi et.al, NEC

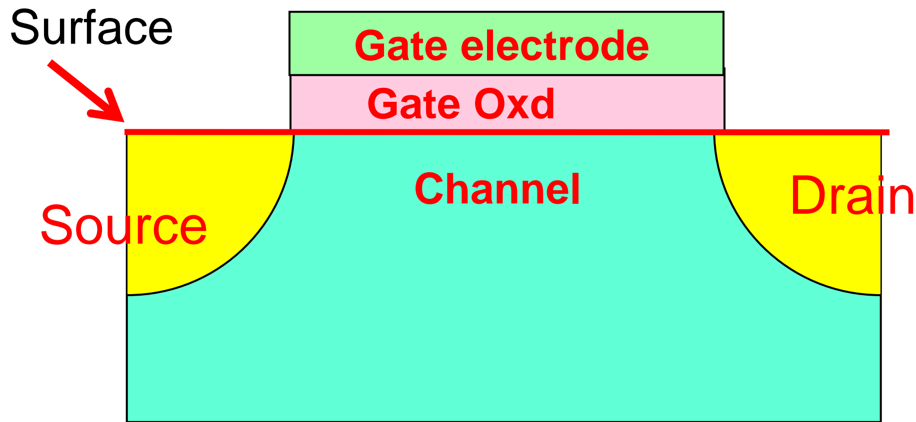
IEDM, 2003



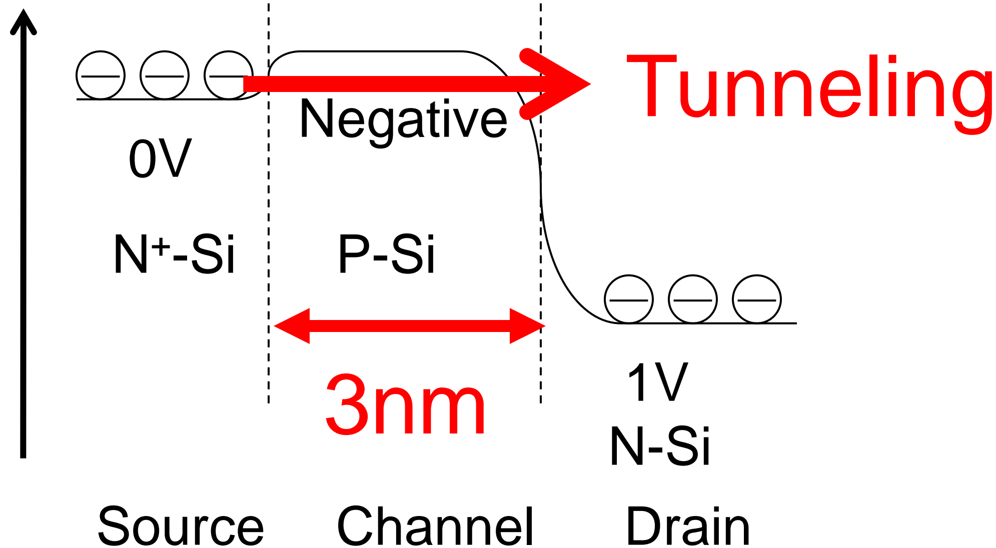


Question:

How far we can go with downscaling?



0 bias for gate

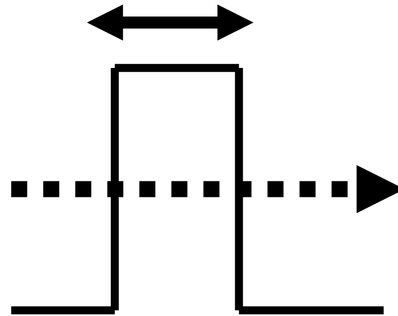


@Vg=0V, Transistor cannot be switched off

Prediction now!

Limitation for MOSFET operation

Tunneling distance



3 nm

Lg = Sub-3 nm?

Below this,
no one knows future!

How far can we go for production?

Past

0.7 times per 3 years

In 40 years: 18 generations, Size 1/300, Area 1/100,000

Now

1970年

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

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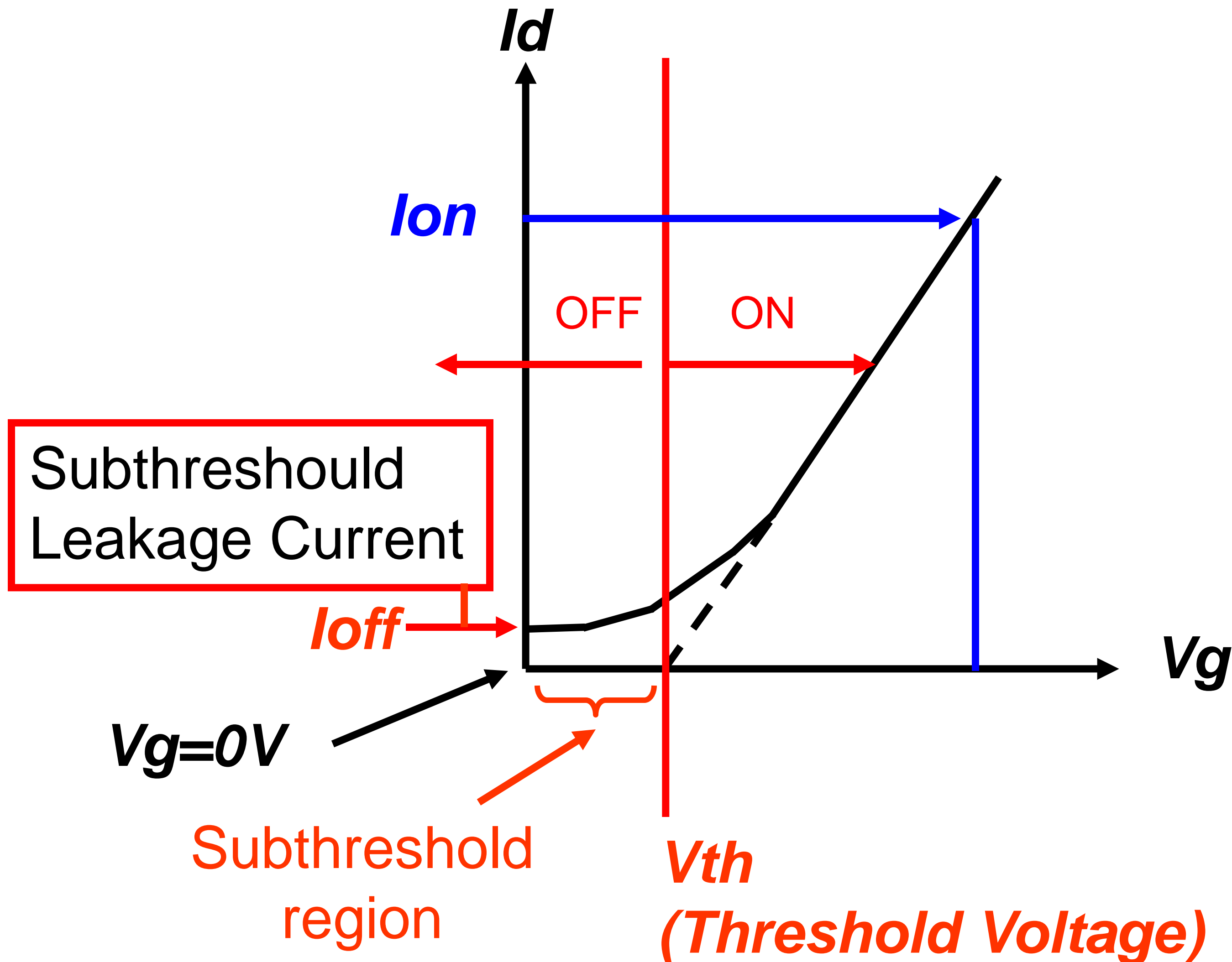
Future

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- **At least 4,5 generations to 8nm**
- **Hopefully 8 generations to 3nm**

Subtheshold leakage current of MOSFET



Vth cannot be decreased anymore

↑

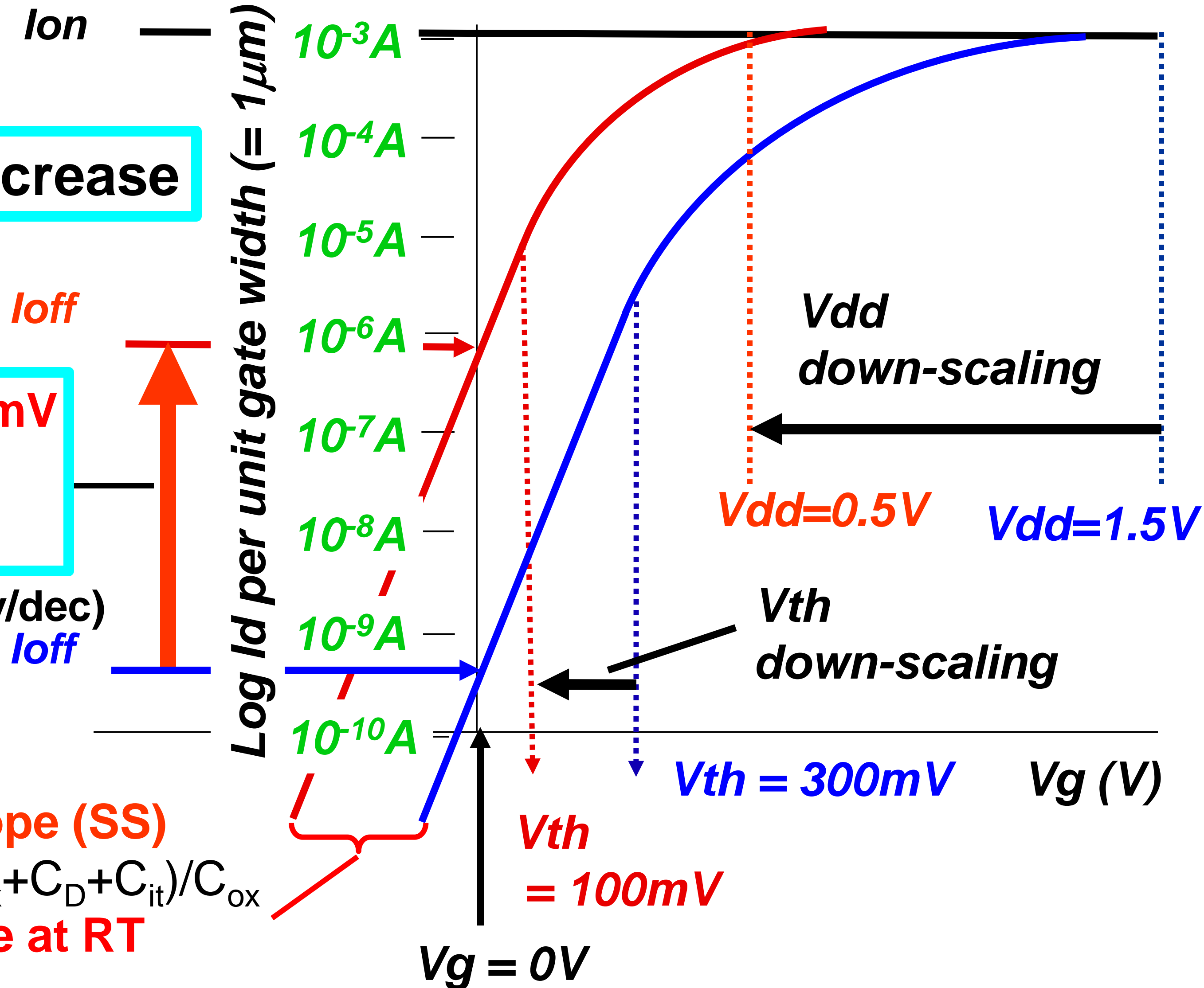
significant Ioff increase

↑

Vth: 300mV → 100mV

Ioff increases with 3.3 decades

(300 – 100)mV/(60mv/dec) = 3.3 dec



Subthreshold slope (SS)

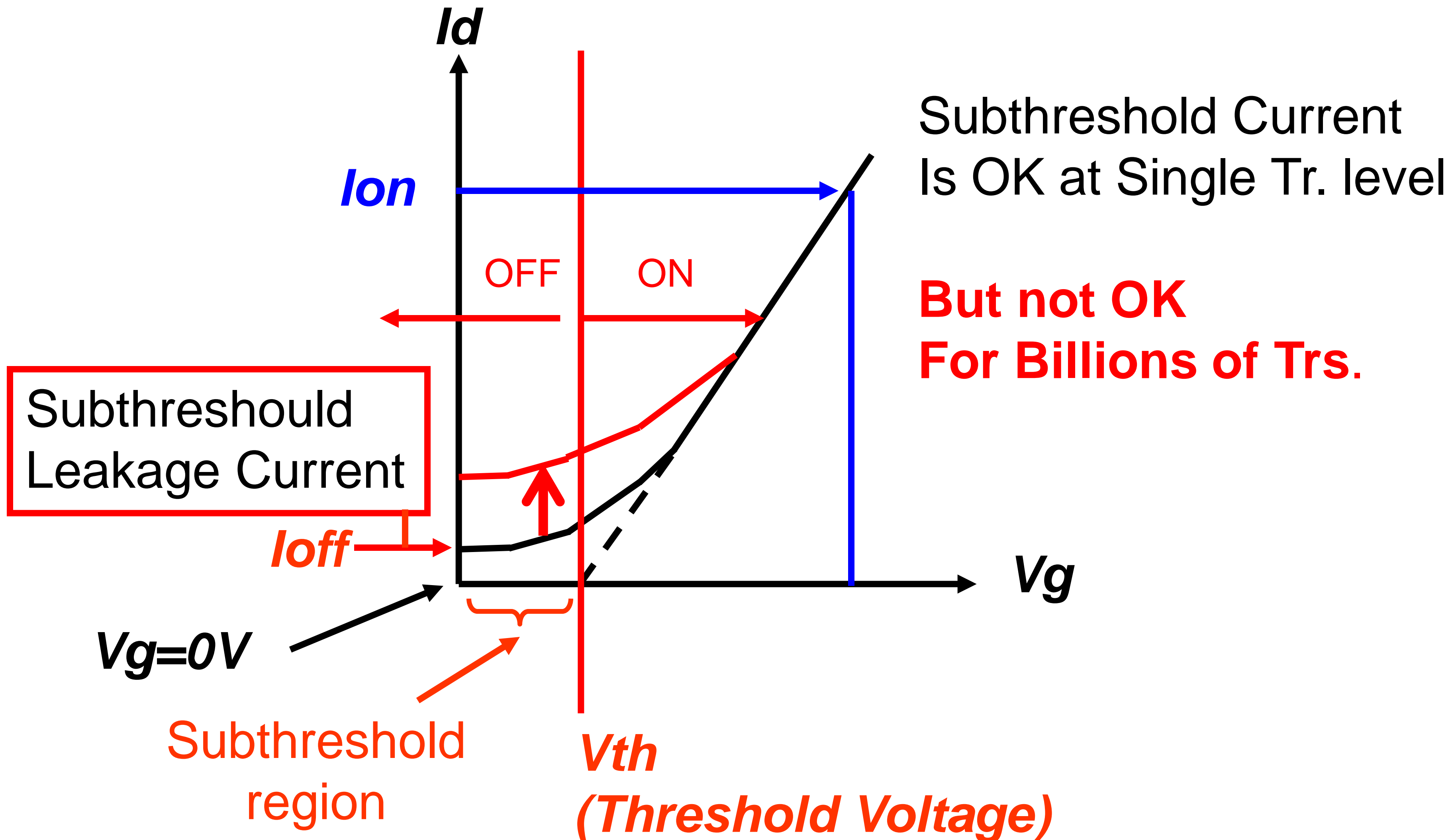
$= (\mathrm{Ln}10)(kT/q)(C_{ox}+C_D+C_{it})/C_{ox}$

$>$ **~ 60 mV/decade at RT**

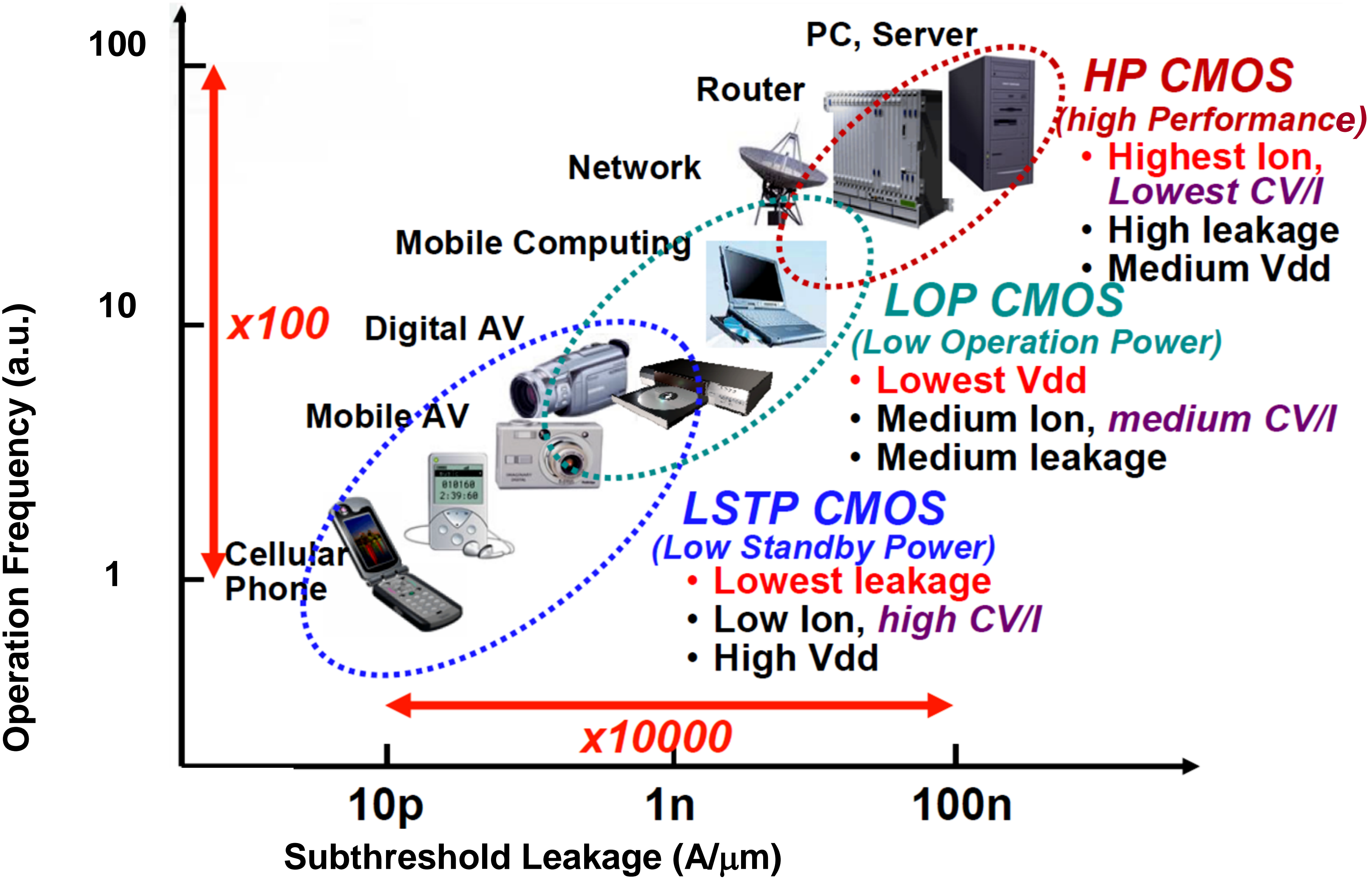
SS value:

Constant and does not become small with down-scaling

Subtheshold leakage current of MOSFET

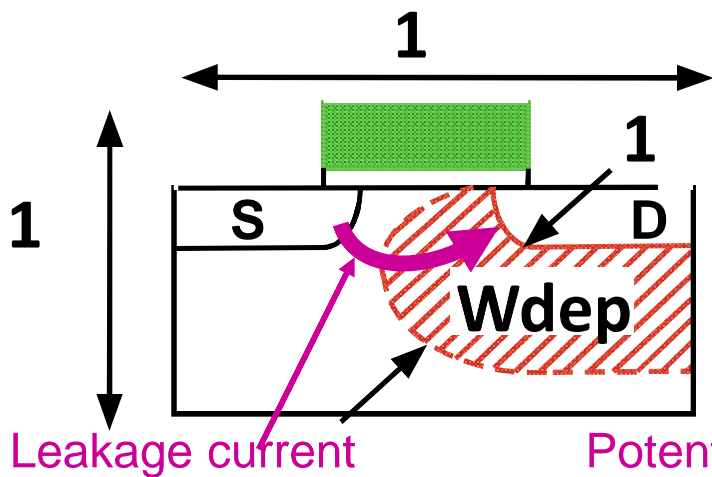


The limit is deferent depending on application



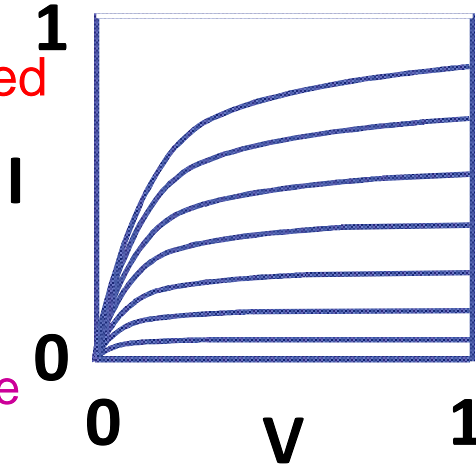
Source: 2007 ITRS Winter Public Conf.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

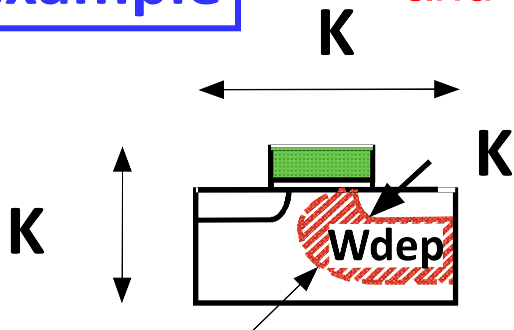
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

X , Y , Z : K,	V : K,	Na : 1/K

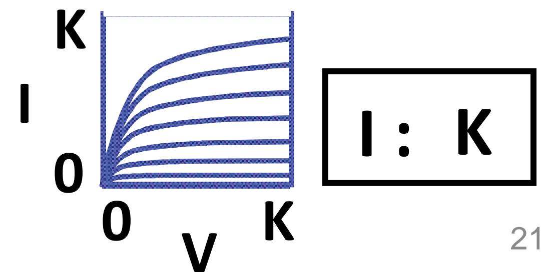
By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$

: K



I : K

Down scaling is the most effective way of Power saving.

The down scaling of MOSFETs is still possible for another 10 years!

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3 important technological items for DS.

New materials

1. Thinning of high-k beyond 0.5 nm
2. Metal S/D

New structures

3. Wire channel